REMARKS/ARGUMENTS

Examiner Britt is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed and amended, and are considered to be in condition for allowance.

Reconsideration of the rejection under 35 USC §101 of Claims 29-42 because the claimed recitation is directed to non-statutory subject matter, is requested in light of the following arguments. Claims 29-42 are amended to claim:

> "A computer implemented hardware design system having a retention device retaining a hardware description coding of a test pattern generation and comparison circuit, which, when executed, automatically creates a physical description of said hardware description coding during an automatic physical design of an integrated circuit for placement on a semiconductor substrate".

The "computer implemented hardware design system" now defines structural and functional interrelationships between the data structure and other claimed aspects of the invention, which permit the data structure's functionality to be realized.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 4, 10, 12, 18, 24, 26, 32, 38, 40, 46, 46, 52, 54, 60, 61, 63, and 67 as

being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments. The claims have been amended particularly point out and distinctly claim the subject matter of the invention. Claims 4, 18, 32, 46, and 61 having the limitation "each subsequent flip circuit" are amended to have "each subsequent flip-flop circuit." Claim 60 is amended to change "parallel-to-parallel" to "parallel-to-serial". The claims with insufficient antecedent basis are amended to insure correct antecedent basis.

Reconsideration of the rejection under 35 USC §102(e) of Claims 1-3, 8-12, 14-17, 22-26, 28, 43-45, 50-54, 56-59, and 62-68 as being anticipated by U.S. Patent 6,249,893 (Rajsuman et al.) is requested in light of the following arguments. Rajsuman et al. does teach testing the microprocessor core by executing its instructions multiple times under pseudo random data and evaluating the results by comparing testing results with simulation results. The Instruction decode logic generates function select and control signals for the instruction execution unit. The starting signal for MISR is delayed to accommodate the latency of pipeline.

However, for claims 1-3, 8-12, 14-17, 22-26, and 28, Rajsuman et al. does not teach to:

a background and command decoder connected to receive test background and command codes from said test controller, to

translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and

a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 1, Lines 4-13; Claim 15, Lines 13-25)

For claims 43-45, 50-54, and 56, Rajsuman et al. does not teach to:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 43, Lines (9-20)

For claims 57-59 and 62-68, Rajsuman et al. does not teach to:

receiving a test pattern command indicating which tests to be performed are communicated to said integrated circuit;

receiving a background pattern code indicating a pattern of multiple bit test stimulus signals to be communicated to said integrated circuit;

decoding said test pattern command and said background pattern code to create said multiple bit test stimulus signals;

adjusting a timing relation of said multiple bit test stimulus signals to provide correct timing relationships for said multiple bit test stimulus signals; and

communicating said multiple bit test stimulus signals to said integrated circuit. (Claim 57, Lines 9-20)

Rajsuman et al. provides decoding of microprocessor instructions not "test pattern command and said background pattern code" that is decoded to create the "multiple bit test stimulus signals" that are applied to a functional integrated circuit. In Rajsuman et al. there is not teaching to adjusting the timing relationship of the "multiple bit test stimulus signals" to provide correct timing relationships required for testing the functional integrated circuit.

Reconsideration of the rejection under 35 USC §103(a) of Claims 7, 21, 49, and 60 as being unpatentable over in U.S. Patent 6,249,893 (Rajsuman et al.) in view of U. S. Patent 6,499,070 (Whetsel) is requested in light of the following arguments.

Briefly, the applicant wishes to point out the major features of the invention, which is a novel apparatus and method using programmable logic/memory commands which are translated into physical logic signals and timings for the logic or memory under test. The results of the test pattern generated and applied to the logic or memory are compared to expected results. The result of the comparison is a pass/fail test result. In addition, the comparison of the expected test response signal with the actual test response signals provides information on the exact location of the failure. Also, since the test pattern generation and comparison circuit architecture is compatible with hardware description languages such as Verilog HDL or VHDL, the test pattern generation and comparison circuit can be automatically generated with a silicon compiler.

Rajsuman et al. does teach testing the microprocessor core by executing its instructions multiple times under pseudo random data and evaluating the results by comparing testing results with simulation results. The Instruction decode logic generates function select and control signals for the instruction execution unit. The starting signal for MISR is delayed to accommodate the

latency of pipeline. Further, Whetsel does teach parallel-to-serial conversion using multiple flip flops (or latches) with a multiplexer circuit. The parallel-to-serial conversion circuits achieves an overlap in serial and parallel operations; providing continuous and concurrent serial to parallel and parallel to serial conversion.

However, for claims 7, 21, 49, and 60 neither Rajsuman et al., nor Whetsel, nor Rajsuman et al. in combination with Whetsel teaches to:

> a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and
>
> a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 1, Lines 4-13, Claim 15, Lines 13-25)

For claim 49 neither Rajsuman et al., nor Whetsel, nor Rajsuman et al. in combination with Whetsel teaches to:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 43, Lines (9-20)

For claims 60, neither Rajsuman et al., nor Whetsel, nor Rajsuman et al. in combination with Whetsel teaches to:

receiving a test pattern command indicating which tests to be performed are communicated to said integrated circuit;

receiving a background pattern code indicating a pattern of multiple bit test stimulus signals to be communicated to said integrated circuit;

decoding said test pattern command and said background pattern code to create said multiple bit test stimulus signals;

adjusting a timing relation of said multiple bit test stimulus signals to provide correct timing relationships for said multiple bit test stimulus signals; and

communicating said multiple bit test stimulus signals to said integrated circuit. (Claim 57, Lines 9-20)

Rajsuman et al. provides decoding of microprocessor instructions not "test pattern command and said background pattern code" that is decoded to create the "multiple bit test stimulus signals" that are applied to a functional integrated circuit. In Rajsuman et al. there is no teaching to adjusting the timing relationship of the "multiple bit test stimulus signals" to provide correct timing relationships required for testing the functional integrated circuit. The serial-to-parallel conversion circuit of Whetsel does not teach decoding "test pattern command and said background pattern code" to create the "multiple bit test stimulus signals" that are applied to a functional integrated circuit. The parallel-to-serial conversion circuit of Whetsel provides continuous and concurrent serial to parallel and parallel to serial conversion, but does not adjust the timing relationship of the "multiple bit test stimulus signals" to provide correct timing relationships required for testing the functional integrated circuit.

The invention as claimed in amended Claims 7, 21, 49, and 60 is believed to be novel and patentable over the combination of Rajsuman et al. in view of Whetsel because there is an insufficient basis, as described above, to conclude

that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. The applicant believes that there is no such basis for the combination. The applicant therefore requests that Examiner Britt reconsider the rejection in view of these arguments.

Reconsideration of the rejection under 35 USC §103(a) of Claims 1, 15, 43, and 57 as being unpatentable over in U.S. Patent 5,617,531 (Crouch et al) in view of U.S. Patent 5,794,175 (Conner) is requested in light of the following arguments.

While Crouch et al. does provide an internal test controller of a data processor and the internal test controller has a test pattern generator that generates a test pattern for each embedded memory of the data processor within the plurality of embedded memories and sequentially provides the test pattern to each embedded memory of the plurality of embedded memories. Conner does provide a system which during testing, will introduce delay in variable amounts into control signals in order to synchronize the control signals.

For Claims 1 and 15, neither Crouch et al., nor Conner, nor the combination of Crouch et al. in view of Conner provides:

> a background and command decoder connected to receive test background and command codes from said test controller, to

translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and

a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 1, Lines 4-13, Claim 15, Lines 13-25)

For claim 43 neither Crouch et al., nor Conner, nor the combination of Crouch et al. in view of Conner provides:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said

multiple bit test stimulus signals as required by said functional integrated circuits. (Claim 43, Lines (9-20)

For claims 60, neither Crouch et al., nor Conner, nor the combination of Crouch et al. in view of Conner provides:

receiving a test pattern command indicating which tests to be performed are "test pattern command and said background pattern code" to create the "multiple bit test stimulus signals" that are applied to a functional integrated circuit. The timing relationship of the "multiple bit test stimulus signals" is adjusted to provide correct timing relationships required for testing the functional integrated circuit. communicated to said integrated circuit;

receiving a background pattern code indicating a pattern of multiple bit test stimulus signals to be communicated to said integrated circuit;

decoding said test pattern command and said background pattern code to create said multiple bit test stimulus signals;

adjusting a timing relation of said multiple bit test stimulus signals to provide correct timing relationships for said multiple bit test stimulus signals; and

communicating said multiple bit test stimulus signals to said integrated circuit. (Claim 57, Lines 9-20)

The combination of Crouch et al. in view of Conner does not teach to a "test pattern command and said background pattern code" that is decoded to create the "multiple bit test stimulus signals" that is applied to a functional integrated circuit. In the combination of Crouch et al. in view of Conner, there is no teaching to adjusting of the timing relationship of the "multiple bit test stimulus signals" to provide correct timing relationships required for testing the functional integrated circuit.

The invention as claimed in amended Claims 1, 15, 43, and 57 is believed to be novel and patentable over the combination Crouch et al in view of Conner because there is an insufficient basis, as described above, to conclude that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. The applicant believes that there is no such basis for the combination. The applicant therefore requests that Examiner Britt reconsider the rejection in view of these arguments.

Reconsideration of the objection to Claims 1-7, 9-21, 23-35, 38-47, 49, 51-56, 59-61, 63, 65, 67, and 68 because of informalities. In the objections to the claims 3 and 4, the applicant believes the use of "wherein" in Line 1 of each claim is indeed a functional term of the form "The test pattern generation and comparison apparatus of claim 1 wherein" that is used in the defining further

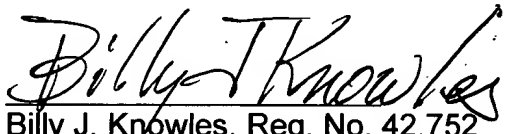
limitations to the claim. In the remaining claims, the claims have been amended to incorporate the corrections requested by the examiner.

The related art references made of record and not relied upon have been reviewed and it is agreed that they do not suggest the present detailed claimed invention.

The applicant acknowledges that claims 4-6, 13, 18-20, 27, 46-48, 55, 61 would be allowable, but are objected to as being dependent upon rejected base claims. In light of the amendments and the above arguments, the applicant respectfully requests that a timely Notice of Allowance for all claims be issued in this case.

It is requested that should Examiner Britt not find that the Claims are now allowable, that the undersigned be called at (845) 452-5863 to overcome any problems preventing allowance.

Respectfully Submitted,
George O. Saile & Associates



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